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Transformerless microinverter for photovoltaic systems

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Abstract
When a galvanic connection between the grid and the PV array is made, a common-mode voltage exists that generates common-mode currents. These common-mode currents may produce electromagnetic interferences, grid current distortion and additional losses in the system. Therefore, to avoid the leakage currents that would penalize the transformerless power chains, it is worth focusing on topologies that do not generate common-mode currents. Some topologies available in the market touch more or less such a crucial requirement. However, some drawbacks generated by the non-utilization of the transformer still exist. These drawbacks maybe reduced or totally eliminated using suitable topologies as well as control strategies. In this paper, a new topology has been developed. Its control strategy has been simulated and experimentally validated. Accordingly, high conversion efficiency and low leakage current level have been demonstrated.

Keywords: Solar PV; Transformerless inverter; Common-mode voltage; Leakage current; Current ripples; Switching control; PWM.

1. Introduction

Nowadays, the invention and development of new energy sources are continuously enhanced because of the critical situation of the chemical industrial fuels such as oil, gas and others. In fact, burning oil, coal and natural gas generates nitrogen oxide, sulphur dioxide, mercury and other toxic metals in the atmosphere, polluting air, land and water. Nuclear fission as an energy source also produces radioactive waste, a material that will remain deadly for thousands of years. The poisonous results of the various pollutants created by the use of these fuels are becoming increasingly harder to justify. This is why the renewable energy sources have become a more important contributor to the total energy consumed in the world. In fact, the demand for solar energy has increased by 20% to 25% over the past 20 years [1]. It is true that the current energy production contribution of photovoltaic (PV) systems is still low, as shown in Figure 1, however, thanks to their continuous cost reduction, efficiency and reliability increase, the market for PV systems is growing worldwide (Figure 2). Currently, solar PV provides some 4800 GW worldwide. Between 2004 and 2009, grid connected PV capacity reached 21 GW and was increasing at an annual average rate of 60% [2]. To enhance the application of PV systems, research activities are being conducted in an attempt to gain further improvement in their cost, efficiency and reliability.

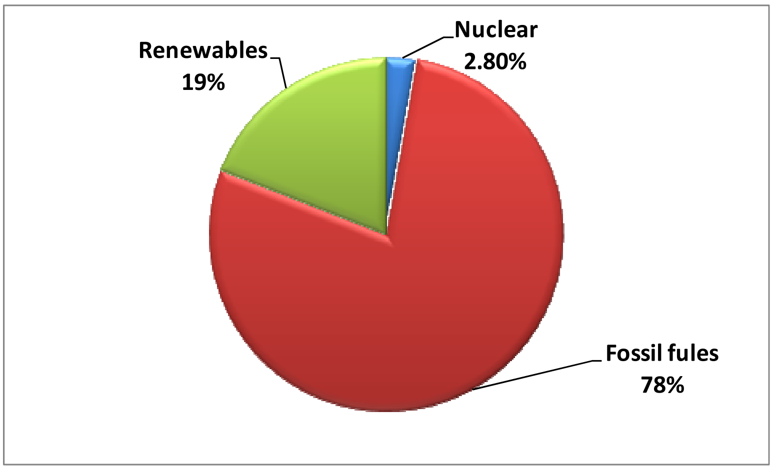

Figure 1. Worldwide electric energy consumption by fuel type for 2008[2]

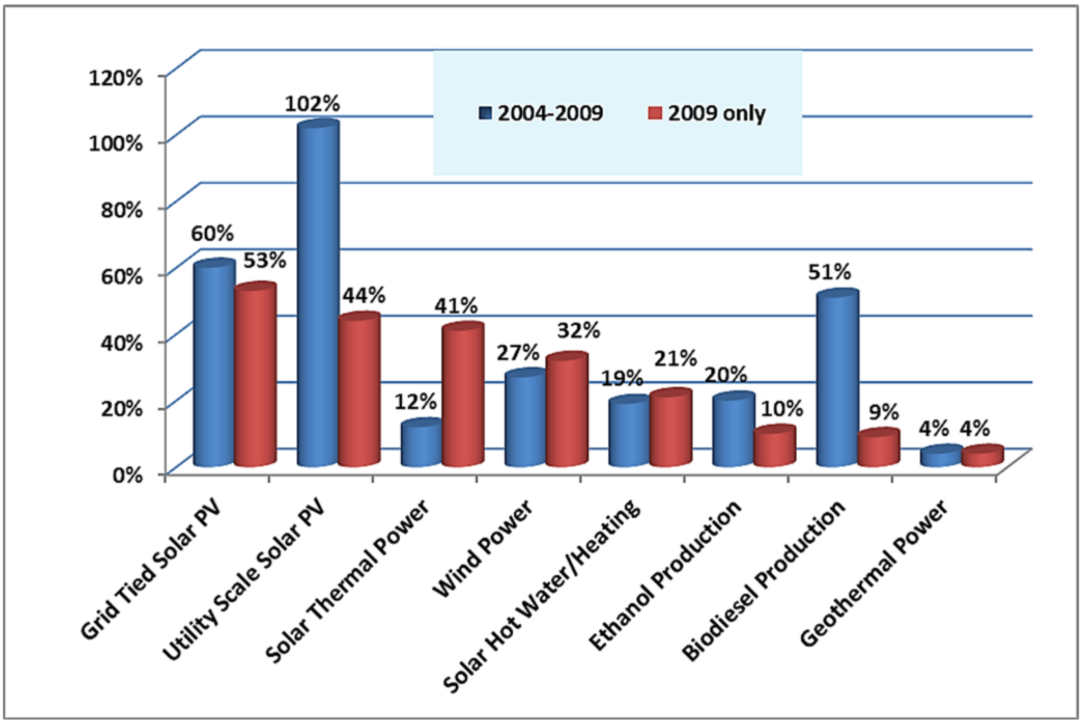

Figure 2. Average annual growth rates of renewable energy capacity for 2004-2009

Early PV systems came in one of two system configurations: string and central [3]. These use long and high voltage DC cables to feed power from the PV array into the inverter and then into the utility grid. These long cables increase power losses. Besides, these configurations mandate the use of single maximum power point tracker (MPPT) for the entire PV system. Because of mismatch losses, the overall system efficiency decreases [4]. Moreover, these configurations necessitate high-level power inverters that minimize and restrict the flexibility of the system to expand.

Recent trends focus on the so-called integrated AC module in which the inverter is enclosed on the back of the panel, whereby, the PV panel is delivered to the user as a complete system. Such a configuration has many advantages. It eliminates DC cables and reduces maximum power point (MPP) mismatch losses. Therefore, it increases the efficiency of the whole system and significantly reduces installation cost.

Since the AC integrated module would be mounted on the back of the solar panel, the transformer that is heavy, bulky, and hard to install should not be a requirement. However, when the transformer is omitted, some drawbacks appear which are due to the galvanic connection between the PV system and the grid. The galvanic isolation can be achieved either on the DC side using a high frequency DC-DC transformer

or on the grid side using low frequency AC transformer. However, PV inverters that have an isolation transformer on the grid side are big in size making the whole system bulky and hard to install. Meanwhile, topologies that use high frequency transformer within the DC-DC converter have a reduced overall efficiency due to the extra losses in the transformer [5-10]. In fact, the elimination of the transformer would allow the increase of the efficiency by 1-2% [4, 11].
However, the transformerless inverter creates a common-mode resonant circuit including the filter, the inverter, the impedance of the grid and the DC source ground parasitic capacitance as illustrated in Figure 3. In this case, a common-mode current is generated and superimposed to the grid, hence increasing its harmonics content [7, 12-16] and causing an electromagnetic interference (EMI) between the PV system and the grid. In addition, the leakage current through the parasitic capacitance can reach considerable levels affecting therefore the safety when a human touches the PV system.

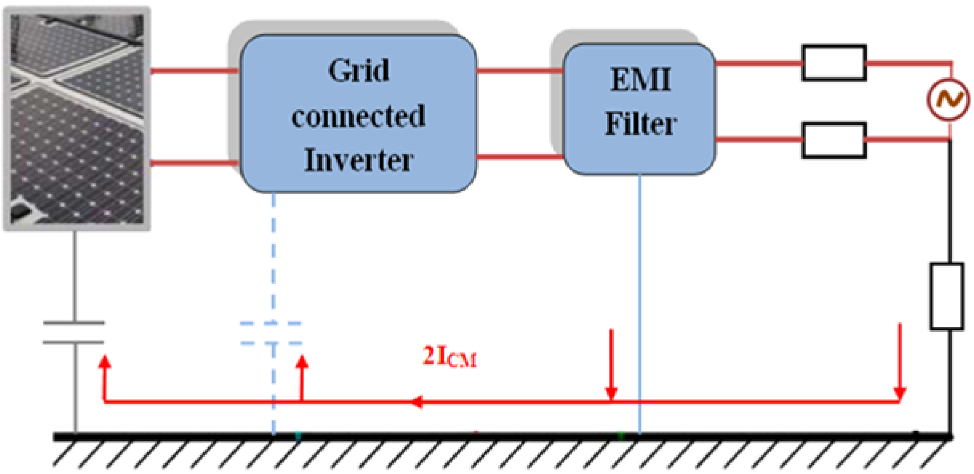

Figure 3. Ttransformerless PV system

To eliminate these currents, topologies that do not generate variant common-mode voltage are necessary for implementing transformerless PV inverters.

2. Common mode voltage description

The common-mode voltage of any circuit is the average of the voltages between the outputs and a common reference. For the full-bridge inverter topology shown in Figure 4, the negative terminal of the DC bus, point N, is used as common reference. Therefore, the common-mode voltage, V_{cm}, is given as:

$$V_{cm} = \frac{v_{AN} + v_{BN}}{2} \tag{1}$$

$$I_{cm} = I_A + I_B = C_{pvg} \frac{dV_{cm}}{dt} \tag{2}$$

The differential mode output voltage, V_{dm}, is the voltage between both outputs:

$$V_{dm} = V_{AN} - V_{BN} = V_{AB} \tag{3}$$

Combining (1) and (3):

$$V_{AN} = \frac{v_{dm}}{2} + V_{cm} \tag{4}$$

$$V_{BN} = -\frac{v_{dm}}{2} + V_{cm} \tag{5}$$

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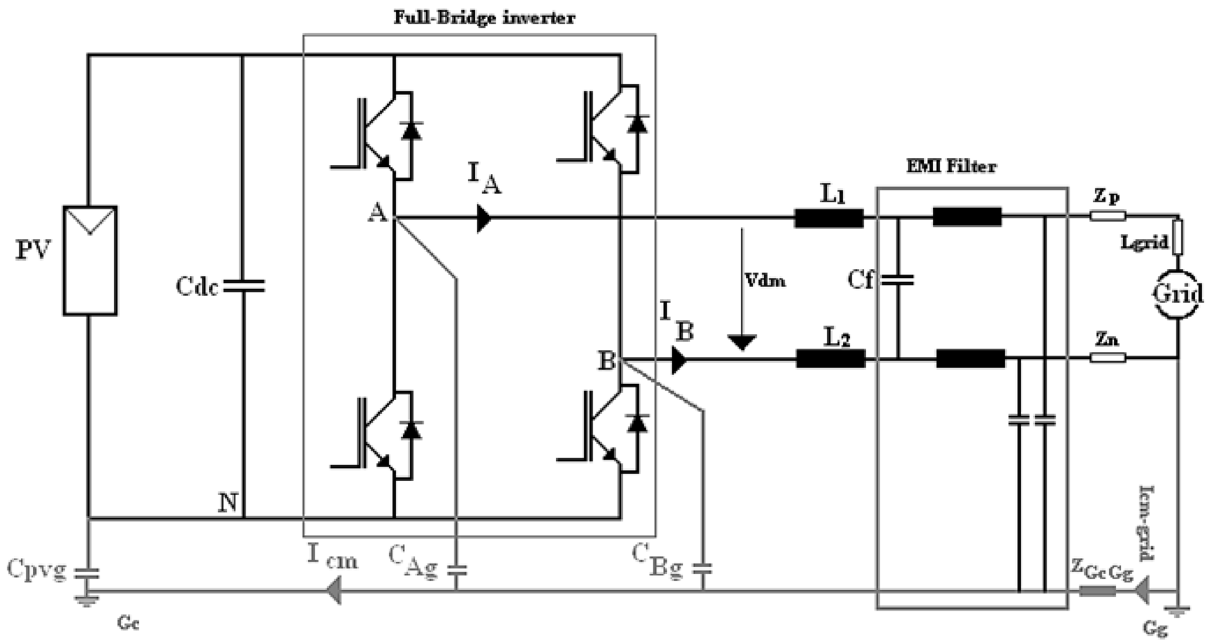

Figure 4. Full-bridge inverter topology with common-mode current path

Based on Figure 4 and equations (1) to (5),two intermediate common-mode models of the full-bridge can be illustrated as shown in Figure 5 and Figure 6, respectively.

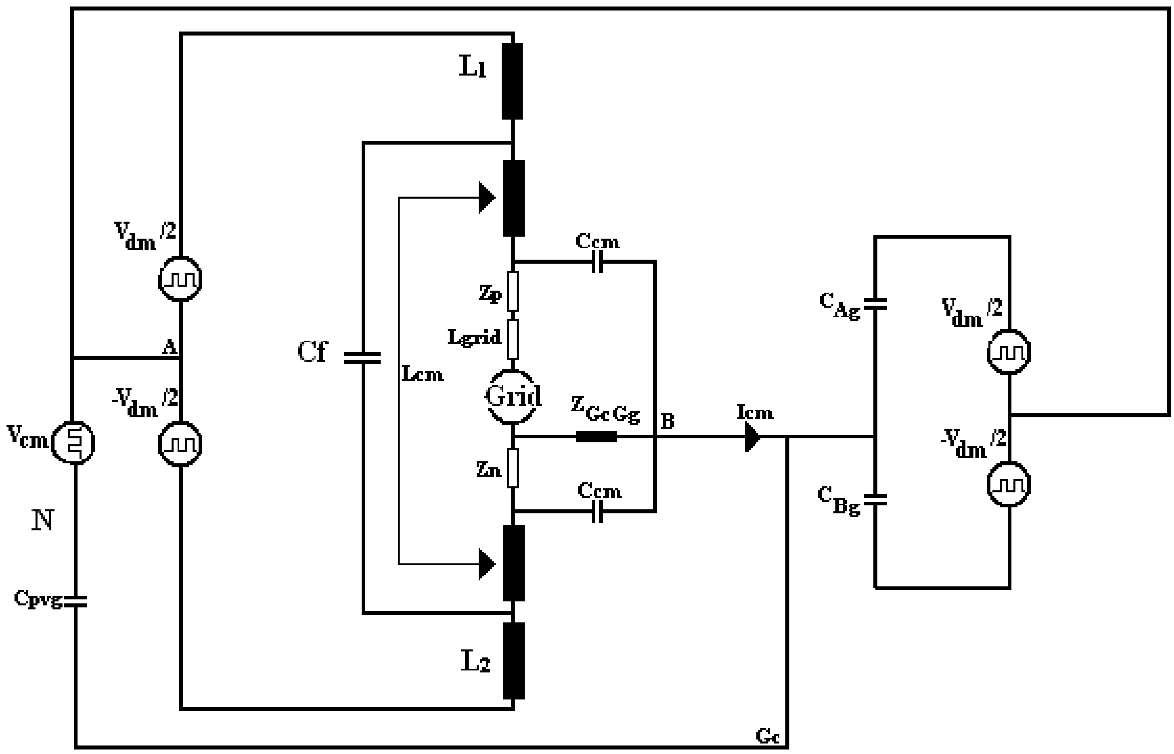

Figure 5.Common-mode voltage model: Initial stage

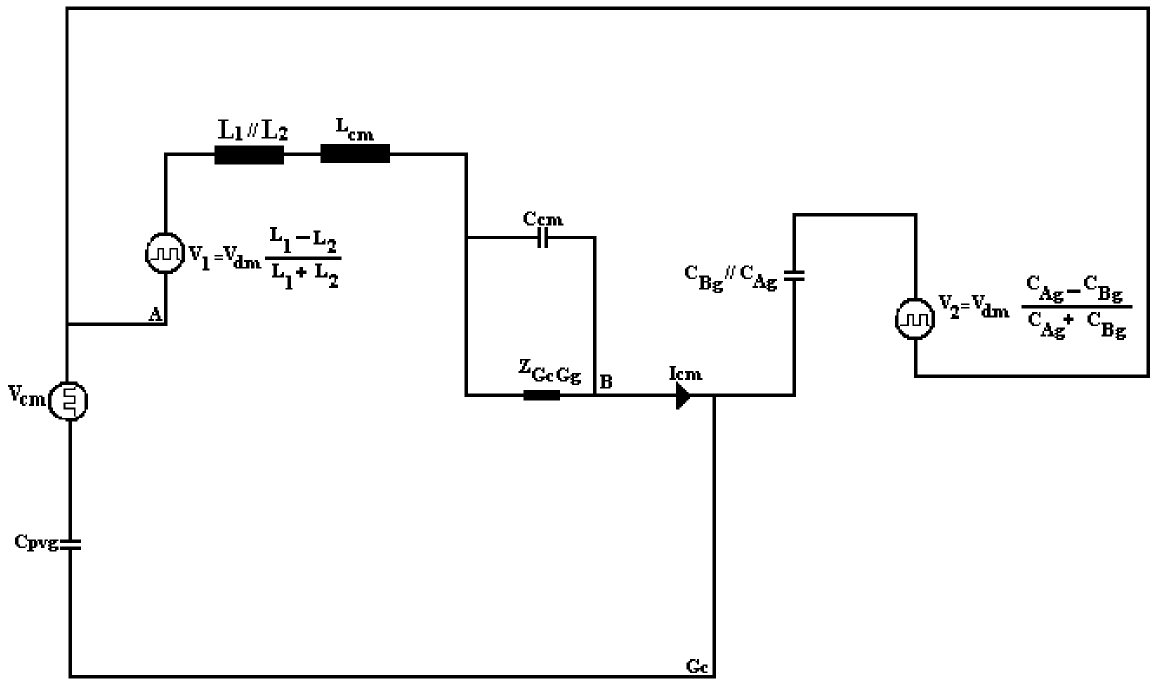

Figure 6. Common-mode voltage model: Intermediate stage

In addition to V_{cm}, the common-mode voltage model includes two sources, V_1 and V_2, which are due to the asymmetries in the differential mode impedances. Therefore, it is possible to have common-mode currents if any impedance asymmetry exists. If the inverter outputs are symmetric, the voltage V_2 is close to zero, which results in neglecting its branch. However, even if the inverter outputs are not symmetric, the influence of V_2 is expected to be much less than V_1 and V_{cm} due to the low values of C_{Ag} and C_{Bg}. Accordingly, the final common mode voltage model of Figure 7 is obtained.
This model includes two sources V_{cm} and V_1 and the total common-mode voltage V_{Tcm}, is:

$$v_{Tcm} = V_{cm} + V_1 \tag{6}$$

V_1 is a function of the asymmetry in the values of inductors L_1 and L_2. Two interesting cases arise. The first is when L_1 and L_2 are identical and equal to ½L. The second case is when L_1=L and L_2=0. For these two cases, V_1 is equal to zero and ½V_{dm}, respectively. Therefore, the common-mode current I_{cm} is found to depend only on V_{cm} and is equal to zero since V_{cm} does not vary with time.

3. Transformerless inverter topology

3.1 Half-bridge

The half-bridge inverter topology, shown in Figure 8 consists of two switches, an inductor L_1 (L_2=0), and an input capacitor divider where its mid-point is connected to the neutral terminal of the grid. This would make the voltage across the parasitic capacitance constant [8, 17, 18].
In this topology, when the upper switch is ON, V_{AB}=½V_{DC}. When the lower switch is ON, V_{AB}=-½V_{DC}. Hence, the total common-mode voltage of the half-bridge is:

$$v_{Tcm} = V_{cm} + v_{dm}\frac{L_2 - L_1}{L_2 + L_1} = v_{BN} = \frac{1}{2}V_{IN} = cte \tag{7}$$

Accordingly, a constant common-mode voltage characterizes the half-bridge. Therefore, no leakage current would appear. However, this topology requires a double DC voltage compared to the full-bridge due to clamping the mid-point of the capacitor divider to the neutral terminal of the grid.

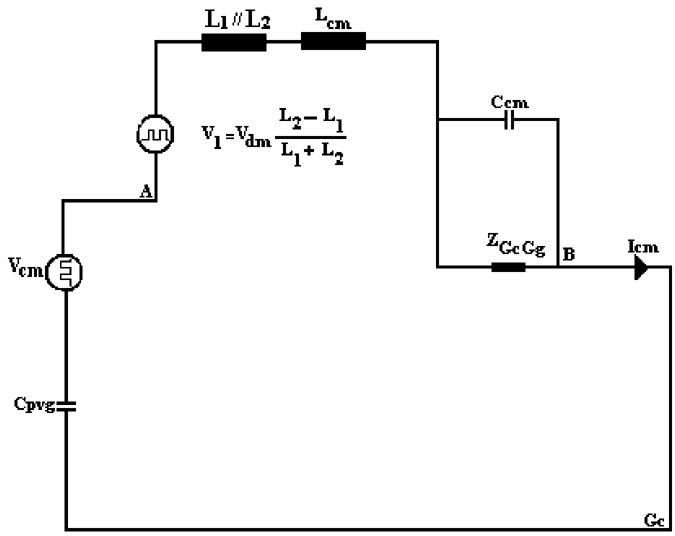

Figure 7.Common-mode voltage model: Final stage

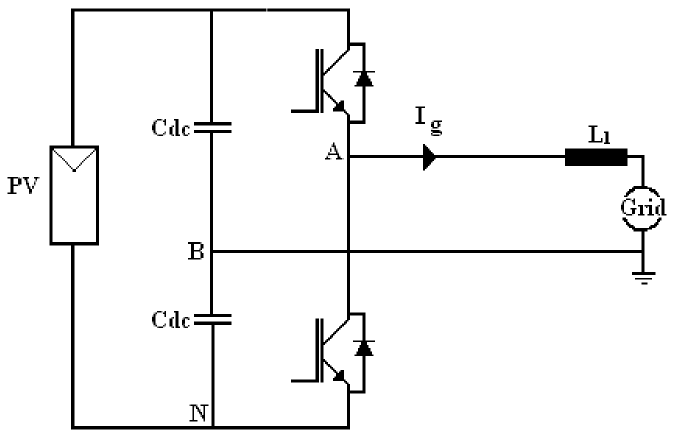

Figure 8. Half-bridge transformerless inverter topology

3.2 Full-bridge

The full-bridge inverter topology of Figure 9 consists of four switches, two output inductors and an input storage capacitor. In this case, $L_2=L_1$ and the total common-mode voltage V_{cm} is $½V_{DC}$.

Conventionally, the full-bridge uses one of two control strategies. For the bipolar PWM control strategy, one group of diagonal switches operates at switching frequency complementary to the other group of switches. As a result, the inverter output voltage has only two levels which results in high current ripple across the output inductors. The major drawback of the full-bridge with bipolar PWM is the high power losses due to two factors. The first is the internal reactive power flow inside the inverter [17]. The second is the double switching frequency required to obtain the same inductor current ripple frequency [12].

The second control strategy that may be applied to the full-bridge is the unipolar PWM. In such modulation, the inverter output voltage has three levels, which decreases significantly the current ripple across the inductors. With this modulation, the inverter has high efficiency due to the absence of the internal reactive power flow. However, with this control strategy, the inverter generates high leakage current level. That is why the full-bridge with unipolar PWM is not popular for transformerless PV systems.

Accordingly, new topologies have to combine the advantages of the bipolar PWM (low leakage current level) and those of the unipolar PWM (High efficiency, low current ripple and three level inverter output voltages). This can be done by adding extra switches to the full-bridge topology. These extra switches would disconnect the PV array from the grid during the freewheeling periods. The most developed topologies are presented and discussed next.

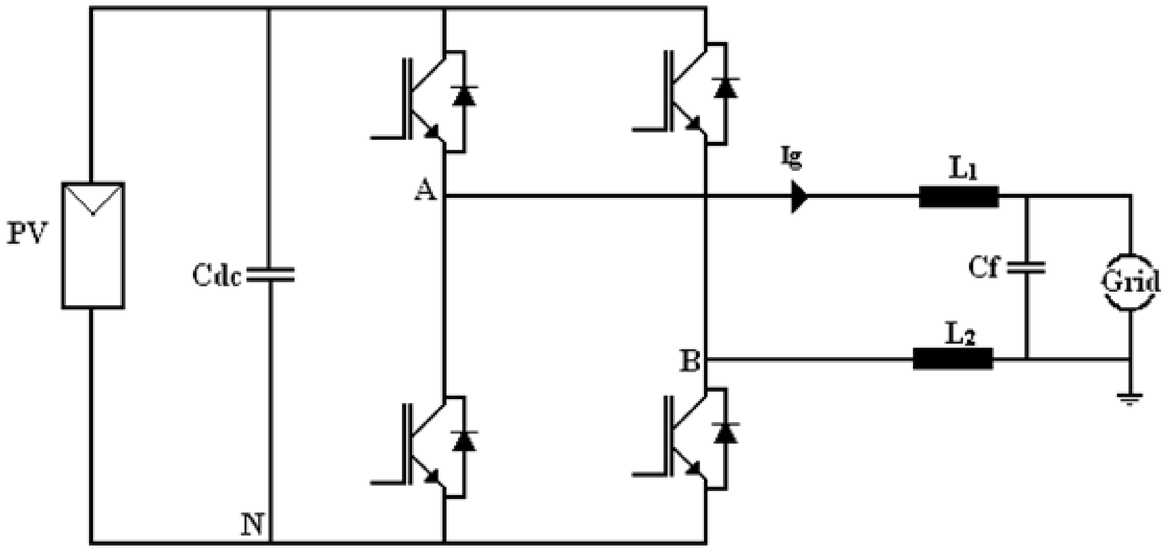

Figure 9. Full-bridge transformerless inverter topology

3.3 H5

This topology, widely described in literature, is an alternative to the full-bridge and includes an extra-switch at the DC side, as shown in Figure 10.

The extra switch is turned OFF at each freewheeling period, during both grid half waves, disconnecting therefore the inverter from the DC source. Besides, with a special control strategy, only the upper switches of the full-bridge form the freewheeling path. With such an implementation, the H5 guarantees a small common-mode voltage variation resulting in a low leakage current level. The main drawback of this topology is that any small mismatch or over delay in the switching process would lead to a high leakage current level [18].

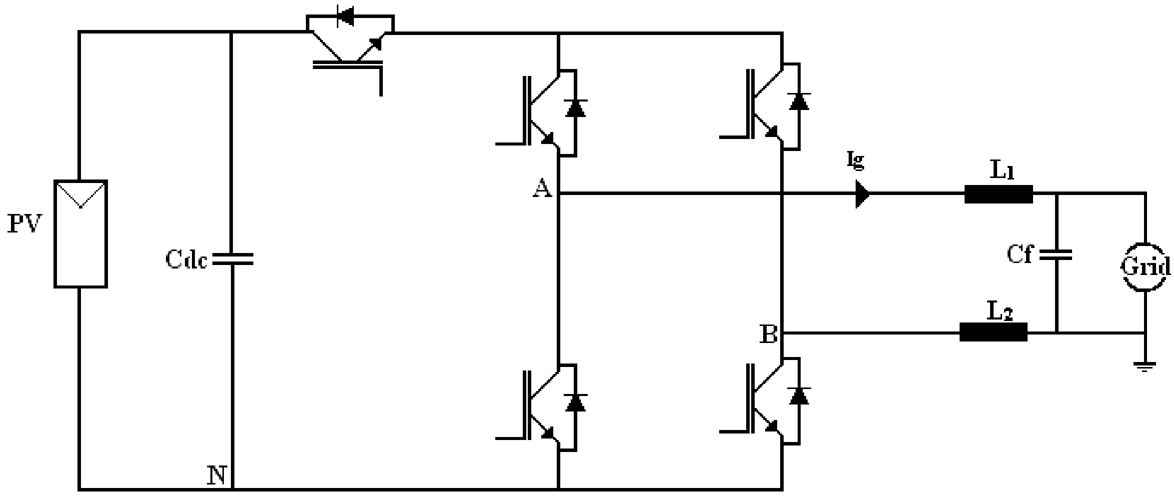

Figure 10. H5 transformerless inverter topology

3.4 H6

This topology, also known as the UniTL topology, has been proposed by [19]. As shown in Figure 11, this topology adds two extra switches compared to the full-bridge. The switching process of this topology is shown in Table 1.

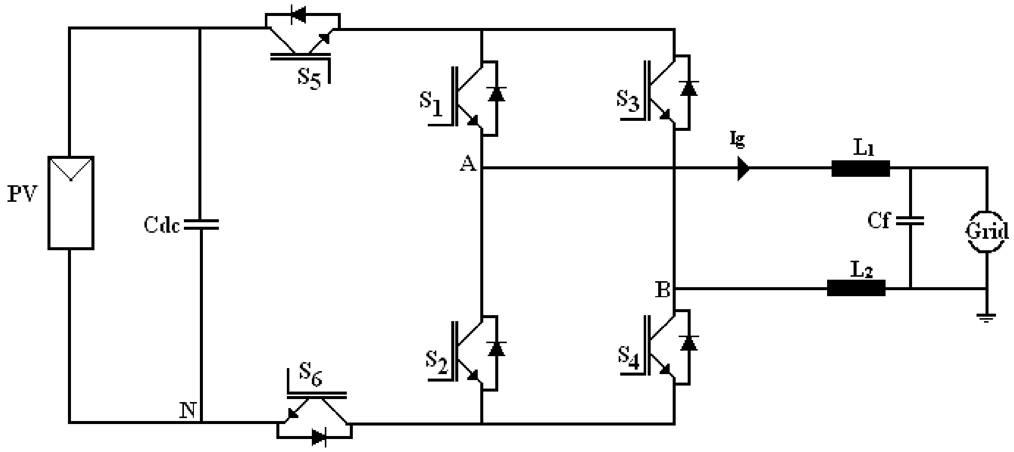

Figure 11. H6 transformerless inverter topology

Table 1. modulation switching strategy of the H6 topology

Switch	Positive half wave	Negative half wave
S_1	x	OFF
S_2	OFF	$\bar{x}$
S_3	OFF	y
S_4	$\bar{y}$	OFF
S_5	$\bar{y}$	$\bar{x}$
S_6	x	y

S_5 is OFF during the high-side freewheeling period, when the current flows through S_1 and the freewheeling diode of S_3, and the common-mode voltage is kept equal to ½V_{DC}. Similarly, the common-mode voltage is the same during the low-side freewheeling period when S_6 is turned OFF.

3.5 HERIC

Still this topology is also based on the full-bridge and uses two extra switches at the AC side (AC bypass). This bypass disconnects the inverter from the grid during each freewheeling period. As shown in Figure 12, either S_5 and the freewheeling diode of S_6 or S_6 and the freewheeling diode of S_5 should be used to form the freewheeling current path. As a result, the internal flow of reactive power is eliminated which helps to increase the entire system efficiency and the occurrence of leakage current is reduced since the common-mode voltage is maintained equal to ½V_{DC}.

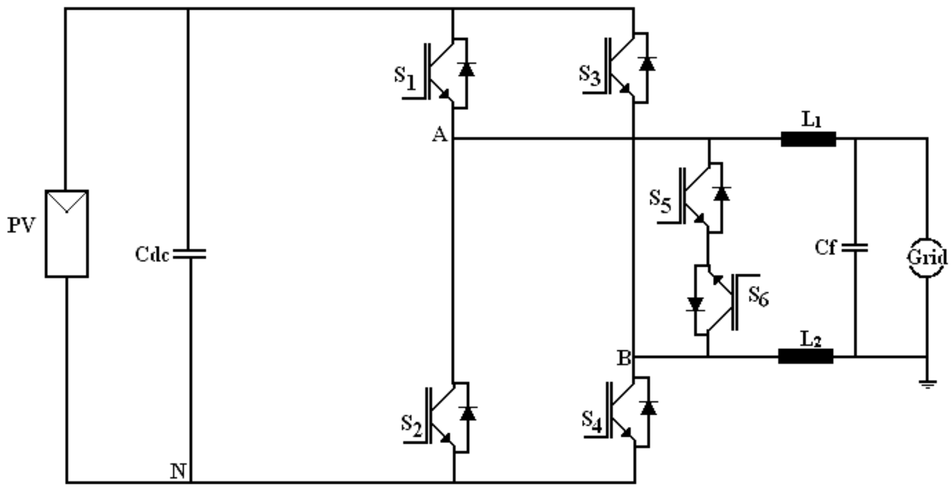

Figure 12. HERIC transformerless inverter topology

4. Proposed topology

The proposed topology, shown in Figure 13, is made up of six switches and one Diode Bridge. With this topology, the inverter is disconnected from the grid each freewheeling period using one switch and two diodes. In fact, during the positive half wave, the freewheeling current finds its path through S_5, D_2 and D_3. During the negative half wave, the freewheeling current flows through S_6, D_1 and D_4. The control strategy of the proposed topology is summarized in Table 2 where *x* and *y* are the PWM control signals.
For this topology, L_1 and L_2 are identical and the total common-mode voltage V_{tcm} depends on V_{cm}. This last is always kept equal to ½V_{DC}.
Based on Table 2, the control strategy applied to the proposed topology has been implemented and compared to the simulation results. The experimental setup and the obtained gates signals are shown in Figure 14 and Figure 15, respectively.

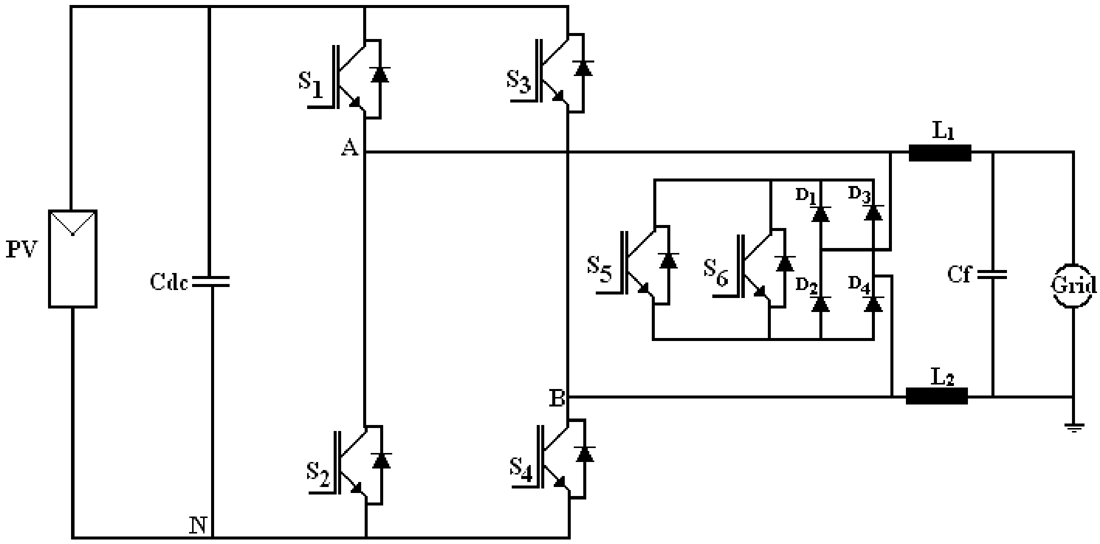

Figure 13. Proposed transformerless inverter topology

Table 2. modulation switching strategy of the proposed topology

Switch	Positive half wave	Negative half wave
S_1	x	OFF
S_2	OFF	y
S_3	OFF	y
S_4	x	OFF
S_5	$\bar{x}$	OFF
S_6	OFF	$\bar{y}$

With this control strategy, the common-mode voltage is kept constant leading to low leakage current level as shown in Figure 16 (a, b,c).
The common-mode voltage variations (Figure 16. a) are very small and the leakage current in Figure 16.b is less than 20mA and it is within the German DIN VDE 0126-1-1Standard of 30mA [10].
For non-ideal components, the estimated efficiency of the proposed topology was 95.14%, which is enough to consider the proposed topology as an attractive alternative for the full-bridge inverter.

Figure 14. Experimental setup of the control strategy applied to the proposed transformerless inverter topology

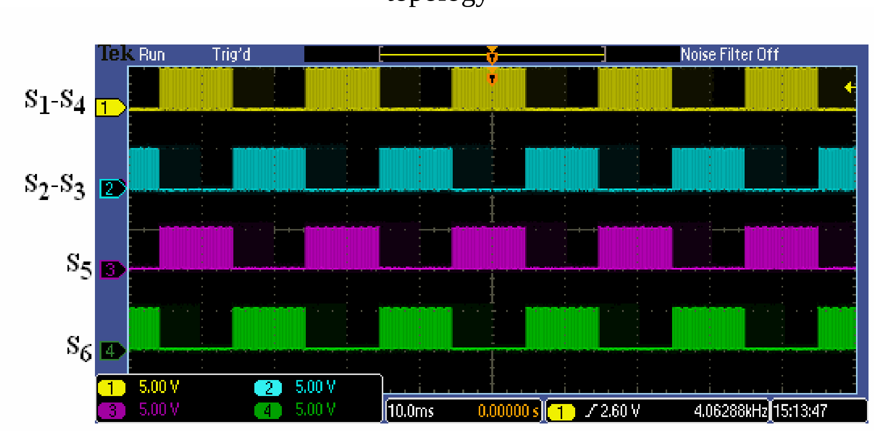

Figure 15. Experimental gates signals applied to the proposed transformerless inverter topology

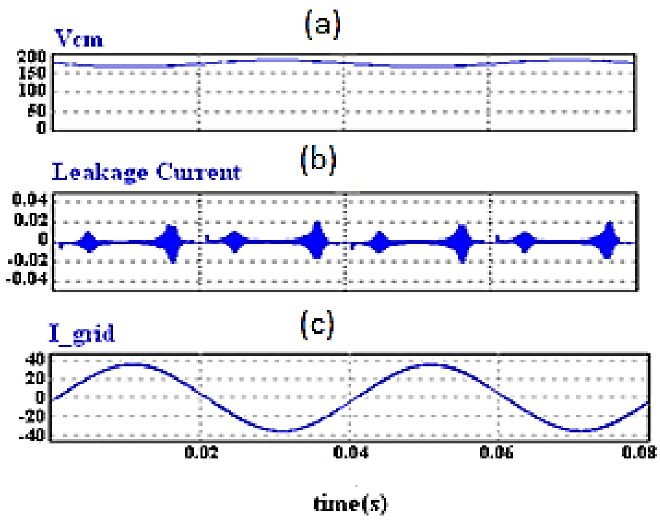

Figure 16. Proposed topology: from top to down, common mode voltage (a), leakage current (b) and grid current(c)

5. Conclusion

Transformerless inverter topologies are being used to overcome the deficiencies of inverters with transformers. The conventional full-bridge which is the basic transformerless topology uses either unipolar or bipolar PWM. The unipolar PWM inverters are characterized by high efficiency. However, they present high leakage current making the entire system unsafe. In the bipolar PWM inverters, the leakage current is very low. However, these inverters suffer from low efficiency due to the double switching losses. The new topology based on disconnecting the PV array from the grid has been developed to combine the advantages of the unipolar and bipolar PWMs. In fact, simulation results show low leakage current within the international Standards mentioned previously. The switching control has been simulated, experimentally validated and applied to this topology. Accordingly, high conversion efficiency low leakage current and small common-mode voltage variations have been demonstrated. Therefore, the proposed topology can be considered as an alternative to the full-bridge based transformerless inverters.

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